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Delay Optimization of Low Power Reversible Gate using MOS Transistor Level design

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ABSTRACT
In Semiconductor industry has witnessed and explosive growth of integration of sophisticated multimedia base application onto mobile electronic gadget since the last decade. The critical concern in this aspect is to reduce the power consumption beyond a certain range of operating frequency. An important factor in the design of VLSI circuits is the choices of reversible logic. Basically conventionally digital circuits have been implemented using the logic gates, which were irreversible in nature only NOT gate are reversible. These irreversible gates produce energy loss due to the information bits lost during the operation information loss occurs because the total number of output signals generated is less than total number of input signals applied. In reversible if the input vector can be uniquely recovered from the output vector and if there is a one to one correspondence between its input and output logic. This paper present a new representation of existing reversible gate in MOS transistor. The MOS transistor designing using a gate diffusion input. Those new representation of MOS transistor has a hoping future in design of low power consumption circuits and high speed application.
Keywords **-** Reversible logic, Garbage Output, Quantum cost, Gate diffusion input, Low Power VLSI.

I. INTRODUCTION

The important factor for the implementation of digital circuit is power consumption. For any electronic gadget the maximum driving time between battery recharge depend on the power dissipation of the electronic system. According to Landauer in logic operation every bit of information loss generates kTln2 joules of heat energy where k is Boltzmann's constant and T is the absolute temperature [1]. Another demonstration of Bennett showed that no energy dissipation would be possible if the circuit consist of reversible gates only [2]. Thus reversibility will be an essential for any latest circuit design. Reversible logic has applications in different areas such as nanotechnology, quantum computing and optical computing etc.

II. BASIC DEFINITIONS, LOGICAL AND PHYSICAL REVERSIBILITY

Definition 2.1: Reversible logic technique preserve one-to-one mapping between inputs and outputs, that logic computation perform almost negligible power dissipation [21].

Definition 2.2: Unused output of reversible logic structure is called as garbage output. More precisely the output which are necessary only to established reversibility condition, are named garbage outputs.

Definition 2.3: In logical reversibility the circuit designer used the gate level approach and satisfy the bijective property between the input and output logic. That fulfil the criteria of logic reversibility.

Definition 2.4: In Physical reversibility can be expressed in a manner of system runs backward without energy loss that system design is physical reversible.

III. MOS TRANSISTOR IMPLEMENTATION OF BASIC REVERSIBLE GATE

There are various reversible gate in the literature among which F2G, TG, FRG and BJN gate are the mostly used reversible gate. In this Subsection show the mostly used gates with function block diagram, quantum implementation and MOS transistor implementation. VLSI CAD tools DSCH-2.7 and microwind are used as simulation and extracting parameters such as delay and power.

3.1 Feynman double gate: Feynman double gate is a 3x3 reversible gate which realize function such as .According to quantum circuit of F2G there are two XOR gate hence the quantum cost of F2G is two. The 6 MOS transistor required for implementation of F2G gate, which is depicted in Figure 1c. If we set input B=C=0 then all output becomes copy of input signal A. The quantum circuit of F2G is depicted in figure 1b.

3.2 Fredkin gate: Fredkin gate had been widely used gate. This gate is one of important feature of preserving the parity of input and output. It is a 3x3 type reversible gate which realize output function such as $P = A, Q = \overline{A}B \oplus AC, R = AB \oplus \overline{A}C$.

According to quantum circuit of Fredkin gate there are four XOR gate, 2 controlled v gate and 1

controlled v+ gate. The 4 MOS transistor required for implementation of FRG gate, which is depicted in figure 3c. This gate is used as a multiplexer.

3.3 Toffoli gate: Toffoli gate is a 3x3 reversible gate which realize output function such as .According to quantum circuit of TG there are two XOR gate, 2 controlled v gate and one controlled v+ gate hence the quantum cost of TG is five. The 6 MOS transistor required for implementation of TG gate, which is depicted in figure 2c. If we set input C=0 then outputs becomes, third output (R) is used for AND gate. The quantum circuit of TG is depicted in figure 2b.

3.4 Peres gate: Peres gate is the combination of Feynman gate and toffoli gate. It is a 3x3 type reversible gate which realize output function such as $P = A, Q = A \oplus B, R = AB \oplus C$. According to quantum circuit of Peres gate there are four XOR gate, 2 controlled v gate and 1 controlled v+ gate. The QC of the Peres gate is 4, and its total logical calculation is 2α+β. The 4 MOS transistor required for implementation of Peres gate, which is depicted in figure 3c.This gate is used as a full adder with minimum quantum cost. Figure indicates the full adder formation.

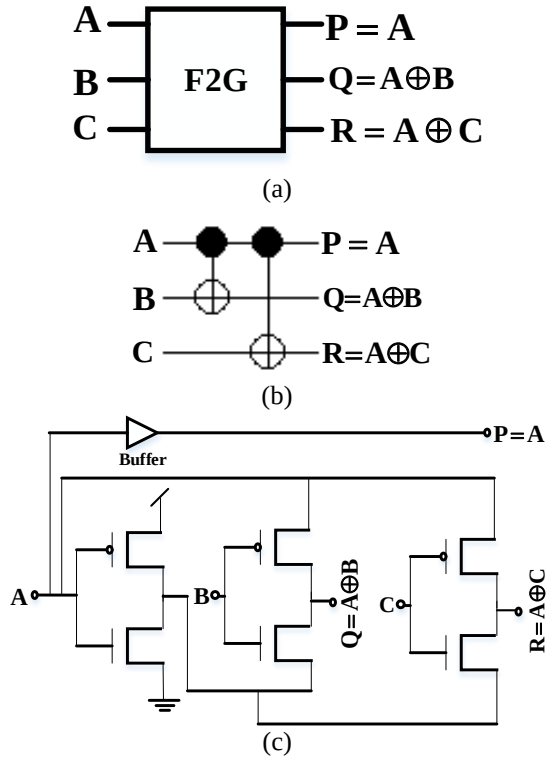


Figure 1 F2G gate (a) Functional diagram (b) Quantum implementation (c) MOS transistor implementation.

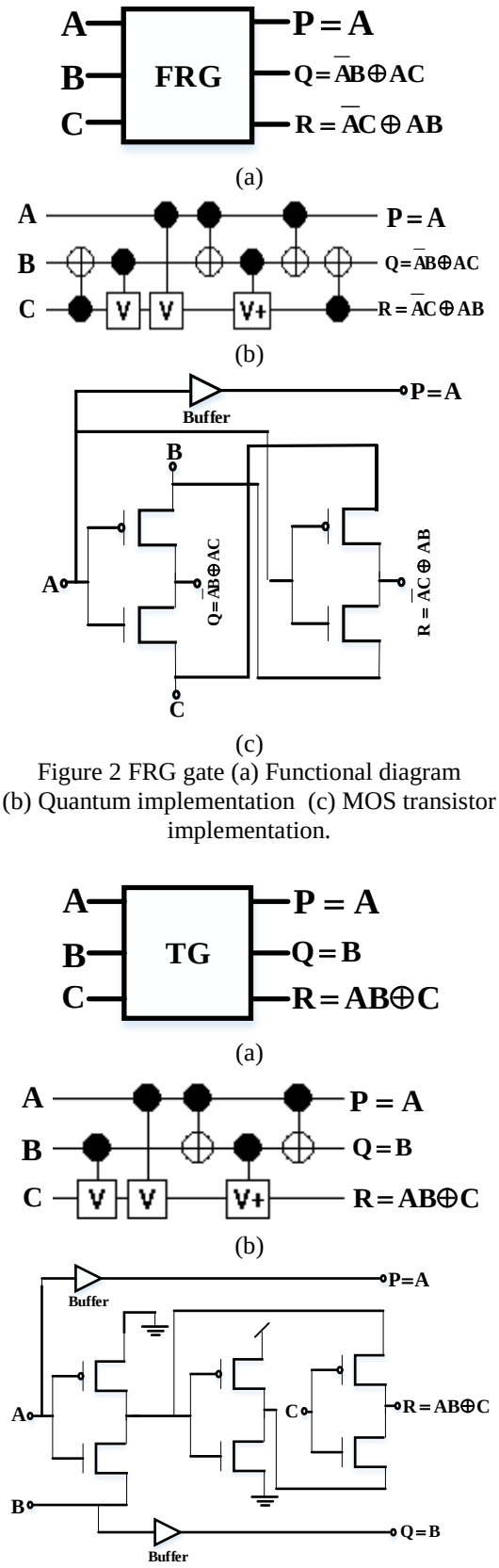


Figure 2 FRG gate (a) Functional diagram (b) Quantum implementation (c) MOS transistor implementation.

Figure 3 Toffoli gate (a) Functional diagram (b) Quantum implementation (c) MOS transistor implementation.

3.5 BJN gate: BJN is a 3x3 type reversible gate which realize output function such as P=A, According to quantum circuit of BJN gat Q=B and $R = (A + B) \oplus C$ .The quantum circuit realized with four XOR gate, 2 controlled v gate and 1 controlled v+ gate. The 4 MOS transistor required for implementation of BJN gate, which is depicted in Figure 3c.This gate is used as a OR when selecting C=0.

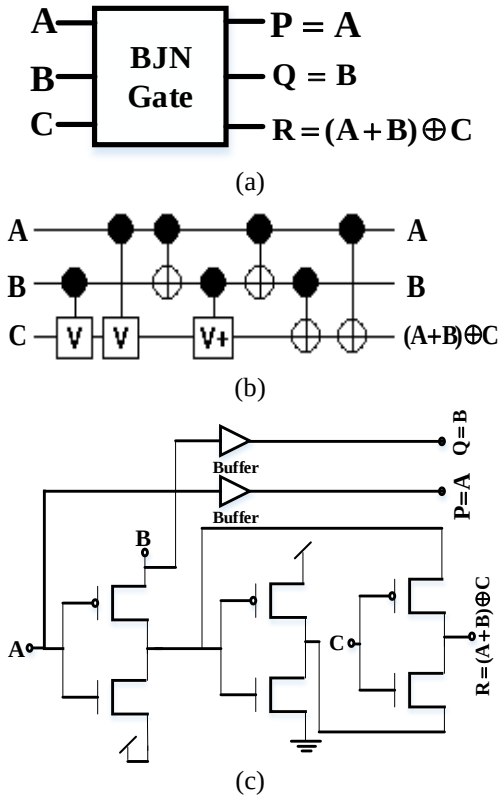
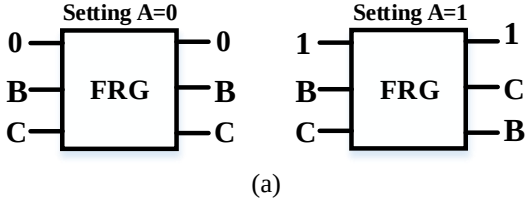


Figure 4 BJN gate (a) Functional diagram (b) Quantum implementation (c) MOS transistor implementation.

IV. UTILITY OF BASIC REVERSIBLE GATE

In this section, we have shown the utility of existing reversible gate. Fredkin gate can be deal with swap second input (B) and third input (C) using first input (A) as a controlled input, i.e it can used as 2:1 multiplexer as depicted in figure. When one input A=1 the other input B and C will be swapped as depicted in figure .Whereas if first input A=0 then all outputs becomes copy the all inputs as depicted in figure.



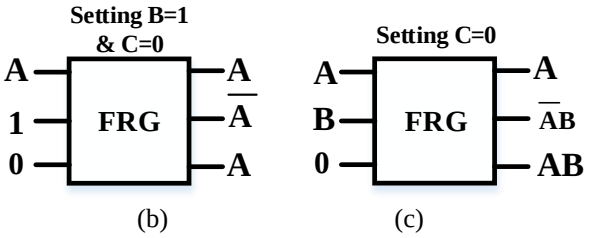


Figure 5. FRG gate utility (a) Signal duplication. (b) Signal duplication and Inverter. (c) Signal duplication and AND operation.

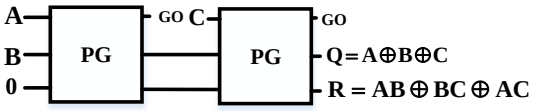


Figure 6 Utility of Peres gate used as full adder.

Feynman gate is used to realize the inverter and signal duplication operation, as depicted in Figure s

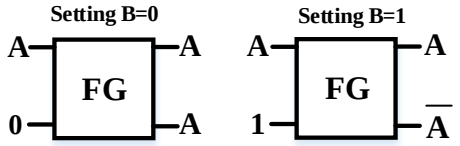


Figure 7 FG used as inverter and signal duplication.

V. RESULT AND DISCUSSION

The result analysis of existing reversible gates, uses the Monte Carlo transient analysis. The each simulation result is perform using the Microwind DSCH simulator. The designs are tested in vast range of temperatures, ranged from 0 to 70^0C are depicted in figure e and f. According to the results of the power and delay analysis that the gates such as FG, FRG, Peres, TG and BJN gate increase approximately in a linear manner. The result are depicted in figure a and b

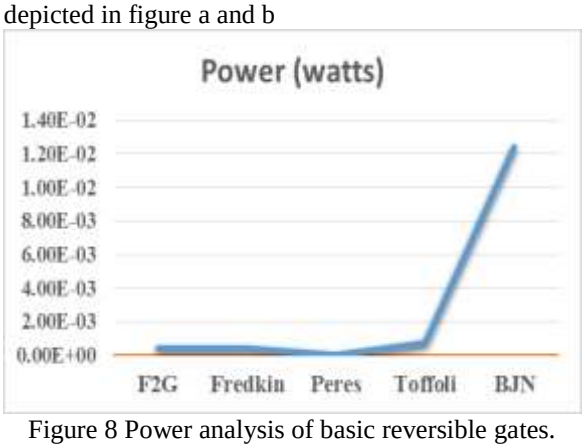


Figure 8 Power analysis of basic reversible gates.

Figure 9 Delay analysis of basic reversible gates.

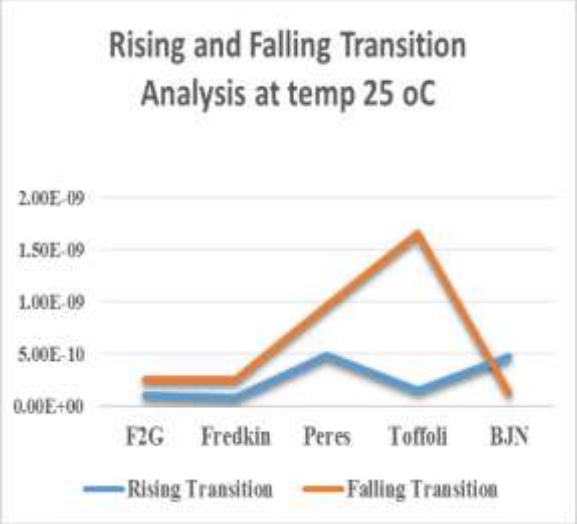


Figure 10 Rising and Falling transition analysis of basic reversible gates.

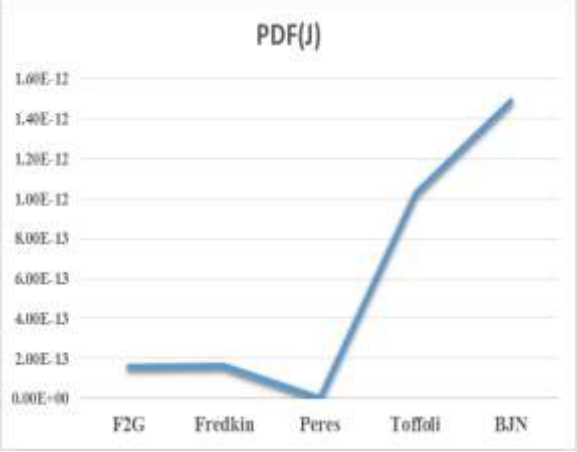


Figure 11 Power delay product of different reversible gates.

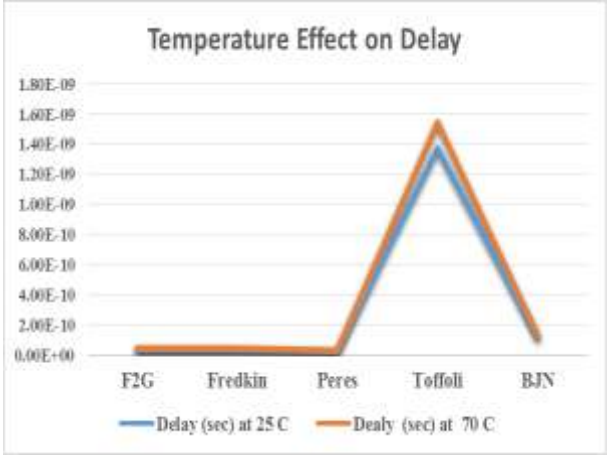


Figure 12 Temperature effect on Delay.

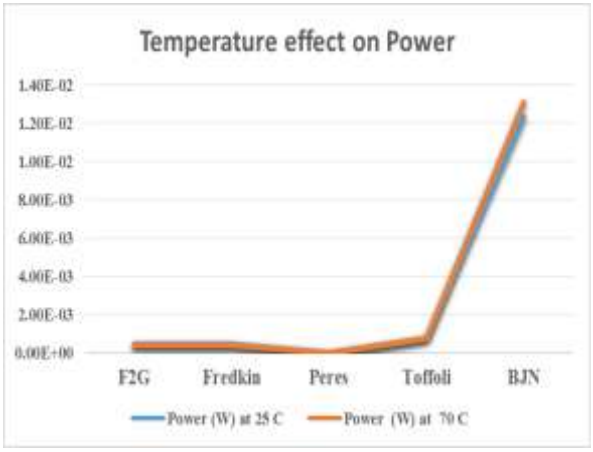


Figure 13 Temperature effect on Power.

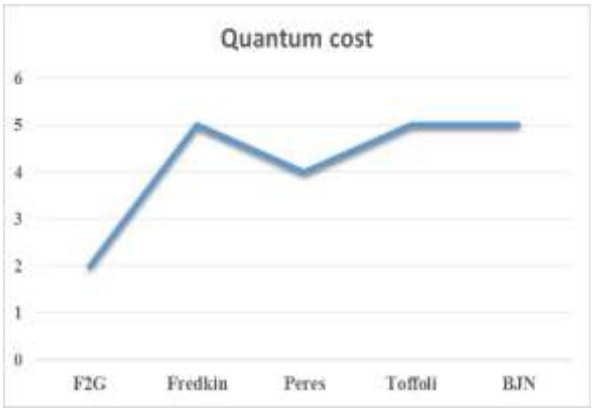


Figure 14 Quantum cost of basic reversible gates.

Table 1 some existing parity preserving reversible gates

Reversible gates	Types	TLC
FRG [14]	3x3	2α+4β+1δ
NFT [12]	3x3	3α+4β+3δ
Islam gate [16]	4x4	3α+3β+1δ
F2G [19]	3x3	2α
MIG [16]	4x4	3α+2β+1δ
NPPRG [15]	4x4	4α+1β
F2PG [15]	5x5	8α+5β+2δ

Table 2 Some existing reversible gates.

Reversible gates	Types	TLC	QC	Parity preserving
FG [13]	2x2	1α	1	No
TG [14]	3x3	1α+1β	5	No
PG [15]	3x3	2α+1β	4	No
FRG [14]	3x3	2α+4β+1δ	5	Yes
F2G [5]	3x3	2α	2	Yes
TR [10]	3x3	2α+1β+1δ	6	No
NG [12]	3x3	2α+2β+3δ	5	No
URG [12]	3x3	2α+1β	7	No
NFT [12]	3x3	3α+4β+3δ	5	Yes
BJN [12]	3x3	1α	5	No
MTSG [17]	4x4	6α+2β	6	No
BME [17]	4x4	4α+3β+1δ	5	No
Inventive0 [18]	4x4	9α+4β+3δ	10	No

VI. CONCLUSION

Reversible logic is low power circuits and no information is lost and have vast applications in the area of low power VLSI, nanotechnology and quantum computing. In this paper the MOS transistor realization of basic reversible gate is done in addition to quantum circuit and total logical calculation. The comparative performance table shows the existing gate superiority with respect to garbage output, quantum cost and total logical calculation. The MOS transistor representation of F2G, TG, and Peres gate are realized using the CAD tool microwind DSCH. The simulation are performed using the 90nm technology. The various parameter extracted during the simulation and the comparative chart shown in this paper.

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